New Software-Designed Instruments

Nicholas Haripersad
Field Applications Engineer
National Instruments
South Africa
Agenda

• What Is a Software-Designed Instrument?
• Why Software-Designed Instrumentation?
• New Software-Designed Instruments
• Software-Designed Instrument… Software
What Is a Software-Designed Instrument?
What Is a Software-Designed Instrument?

Typical Modular Instrument

Software

Processor

Fixed FPGA Firmware

Hardware

Identical hardware architecture and measurement quality

Software-Designed Instrument

Processor

FPGA

Out-of-the-box functionality with FPGA enhancements
Out-of-the-Box Functionality + FPGA Enhancements

- I/O
- Calibration
- DSP
- Triggering
- Acquisition

Synchronization

Application-Specific Enhancement
The NI Approach

We call this the LabVIEW Reconfigurable I/O (RIO) architecture.

Highly Productive LabVIEW Graphical Programming Environment for Programming Host, FPGA, I/O, and Bus Interfaces
FPGA Technology

Memory Blocks
Store data sets or values in user defined RAM

Configurable Logic Blocks (CLBs)
Implement logic using flip-flops and LUTs

Multipliers and DSPs
Implement signal processing using multiplier and multiplier-accumulate circuitry

I/O Blocks
Directly access digital and analog I/O

Programmable Interconnects
Route signals through the FPGA matrix
Program with LabVIEW FPGA

- Familiar LabVIEW programming elements
- Develop, simulate, debug, compile and deploy through LabVIEW
- Integrate external FPGA IP

High-Performance Features

- High-throughput math functions
- Advanced timing control with Single Cycle Timed-Loops
- Access to optimized DSP Cores

Access to IO and Peripherals

- Simple API for front-panel IO
- High bandwidth streaming over PCI Express to Host or other PXI devices
- Random access read/write to DRAM
Why Software-Designed Instrumentation?

– and –

New Software-Designed Instruments
Why FPGAs for Instruments?

- **High-Throughput Processing**
  - Inherently parallel
  - High clock rate
  - Algorithm-specific pipelining

- **Low-Latency Decision Making**
  - Custom logic in a single clock cycle

- **Complete Determinism**
  - Design implemented in a custom circuit

- **Reprogrammable Logic**
  - Design can be updated while system is running
User-Programmable FPGAs on Software-Designed Instruments Enable:

1. On-FPGA Measurements and Stimulus Generation
2. Closed-Loop or Protocol-Aware Test
3. Custom Triggering and Data Reduction
4. Deterministic Test Execution and DUT Control
5. Application-Specific Personalities

Higher Test Throughput  Hardware Re-Use and Future-Proofing  New, Innovative Tests

Lower Total Cost of Test

ni.com
1. On-FPGA Measurements and Stimulus Generation

- Higher Test Throughput
- Hardware Re-Use and Future-Proofing
- New, Innovative Tests

Lower Total Cost of Test

ni.com
# 26.5 GHz Vector Signal Analyzer

![Image of the 26.5 GHz Vector Signal Analyzer](image-url)

## PXIe-5668 Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Frequency Range</strong></td>
<td>20 Hz to <strong>26.5 GHz</strong></td>
</tr>
<tr>
<td><strong>Analysis BW</strong></td>
<td>320 MHz below 3.6 GHz</td>
</tr>
<tr>
<td></td>
<td>765 MHz above 3.6 GHz</td>
</tr>
<tr>
<td><strong>Phase Noise</strong></td>
<td>-129 dBC/Hz at 1 GHz</td>
</tr>
<tr>
<td>(Typ, @10kHz offset)</td>
<td></td>
</tr>
<tr>
<td><strong>Noise Floor</strong></td>
<td>&lt;=-145 dBm/Hz (26 GHz)</td>
</tr>
<tr>
<td><strong>TOI</strong></td>
<td>&gt;=+20 dBm (26 GHz)</td>
</tr>
<tr>
<td><strong>New Features</strong></td>
<td>Kintex-7 410T FPGA</td>
</tr>
<tr>
<td></td>
<td>Programmable with LabVIEW</td>
</tr>
<tr>
<td><strong>Slots</strong></td>
<td>7</td>
</tr>
</tbody>
</table>
# 2 GHz Reconfigurable IF-Digitizer

## PXie-5624R Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sample Rate</td>
<td>2 GS/s</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>12-bit</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
<td>2 GHz</td>
</tr>
<tr>
<td>New Features</td>
<td>Kintex-7 410T FPGA Programmable with LabVIEW PCI Express x8 Gen 2 bus interface (&gt; 3 GB/s)</td>
</tr>
<tr>
<td>Slots</td>
<td>1</td>
</tr>
</tbody>
</table>
Real-Time Spectrum Analysis

Features

• Gapless persistence, spectrogram, and trace statistics (max hold, min hold, average) calculated on FPGA
• Ability to process up to 2 M FFTs/s using overlapped, windowed FFTs
• Real-time frequency mask triggering
• 100% probability of intercept (POI) minimum duration options:
  • 1 µs or >15 µs
Demo: Real-Time Spectrum Analysis

- PXIe-5668R VSA + PXIe-7976R FlexRIO in PXIe-1085
  - May use other P2P-capable RF analyzers
- Up to 800 MHz RF bandwidth (3 GB/s)
2. Closed-Loop or Protocol-Aware Test

Higher Test Throughput  Hardware Re-Use and Future-Proofing  New, Innovative Tests

Lower Total Cost of Test
High-Speed Serial Instruments

PXle-6591R & PXle-6592R Specifications

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-speed serial interface</td>
<td>Up to 12.5 Gbps&lt;br&gt;Up to 8 TX and RX lanes</td>
</tr>
<tr>
<td>Connector</td>
<td>SFP+ or Mini-SAS HD</td>
</tr>
<tr>
<td>RAM</td>
<td>2 GB / 10.6 GB/s bandwidth</td>
</tr>
<tr>
<td>FPGA</td>
<td>Kintex-7 410T FPGA&lt;br&gt;Programmable w/ LabVIEW&lt;br&gt;PXI Express x8 Gen 2 bus interface (&gt; 3 GB/s)</td>
</tr>
</tbody>
</table>

Examples for:
- JESD204B
- Xilinx Aurora
- Serial RapidIO
- 10 Gigabit Ethernet
- CPRI

“FlexRIO-like” VHDL control of Xilinx MGTs
3. Custom Triggering and Data Reduction

- Higher Test Throughput
- Hardware Re-Use and Future-Proofing
- New, Innovative Tests

Lower Total Cost of Test
### PXle-5171R Specifications

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channels</td>
<td>8 (simultaneously sampled)</td>
</tr>
<tr>
<td>ADC</td>
<td>250 MS/s, 14-bit</td>
</tr>
<tr>
<td>Analog Bandwidth</td>
<td>250 MHz</td>
</tr>
<tr>
<td></td>
<td>Selectable 100 MHz filter</td>
</tr>
<tr>
<td>Input ranges</td>
<td>0.2 (V_{pp}) to 5 (V_{pp})</td>
</tr>
<tr>
<td>ENOB</td>
<td>(&gt; 11) (preliminary)</td>
</tr>
<tr>
<td>RAM</td>
<td>1.5 GBit</td>
</tr>
<tr>
<td>FPGA</td>
<td>Kintex-7 410T FPGA</td>
</tr>
<tr>
<td></td>
<td>Programmable with LabVIEW</td>
</tr>
<tr>
<td></td>
<td>PXI Express x8 Gen 2 bus interface (&gt; 3 GB/s)</td>
</tr>
<tr>
<td>No. of Slots</td>
<td>1</td>
</tr>
</tbody>
</table>
Detect Events Faster and Deterministically

Only some events get captured.

Continuous acquisition and processing without dead time capturing all events.
4. Deterministic Test Execution and DUT Control

Higher Test Throughput

Hardware Re-Use and Future-Proofing

New, Innovative Tests

Lower Total Cost of Test

ni.com
# PXIe-5646R Specifications

<table>
<thead>
<tr>
<th>Configuration</th>
<th>VSA and VSG with independent LOs 24 DIO lines</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>65 MHz to 6 GHz</td>
</tr>
<tr>
<td>Sample Rate</td>
<td>250 MS/s</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>200 MHz</td>
</tr>
<tr>
<td>Features</td>
<td>• Virtex-6 LX240T programmable FPGA w/ LabVIEW</td>
</tr>
<tr>
<td></td>
<td>• Fast Tuning Mode: &lt;400 μs</td>
</tr>
<tr>
<td>New Features</td>
<td>• Support for 802.11ac 160 MHz</td>
</tr>
<tr>
<td></td>
<td>• Support for LTE-Advanced</td>
</tr>
</tbody>
</table>

6 GHz, 200 MHz Bandwidth Vector Signal Transceiver
Test Sequencing

Software-Based Test Sequencing

Hardware-Based Test Sequencing

Hardware-Based Test Sequencing with FPGA
5. Application-Specific Personalities

Higher Test Throughput

Hardware Re-Use and Future-Proofing

New, Innovative Tests

Lower Total Cost of Test
Multiple Personalities

**DUT A**
- Serial RapidIO
- 1 Lane
- 3.125 Gbps

**DUT B**
- Serial RapidIO
- 4 Lanes
- 6.25 Gbps
User-Programmable FPGAs on Software-Designed Instruments Enable:

1. On-FPGA Measurements and Stimulus Generation
2. Closed-Loop or Protocol-Aware Test
3. Custom Triggering and Data Reduction
4. Deterministic Test Execution and DUT Control
5. Application-Specific Personalities

Higher Test Throughput  Hardware Re-Use and Future-Proofing  New, Innovative Tests

Lower Total Cost of Test
Software-Designed Instrument.... *Software*
Software-Designed Instrument Programming Options

Instrument Driver
- Industry-standard programming paradigm
- Out-of-the-box functionality

Instrument Driver FPGA Extensions
- Industry-standard programming paradigm
- Out-of-the-box functionality
- Application-specific FPGA enhancements

LabVIEW Sample Projects and Instrument Design Libraries
- Variety of architectural templates
- End-to-end customization of processor and FPGA capabilities

Maximum Compatibility

Maximum Flexibility
Instrument Drivers

- Primary Benefit: Hardware Abstraction
  - APIs for simplified instrument programming
    - LabVIEW API
    - C/C++ and .NET APIs
  - Code portability
    - Across driver versions
    - Across hardware devices
    - Across vendors (IviScope, IviDMM)

- NI Instrument Drivers Add:
  - Configuration in NI MAX
  - Soft front panels (SFPs) for interactive use
  - Example programs that exercise full functionality of the API
  - Integrated API help/documentation
The compatibility of industry-standard instrument drivers

The flexibility of the LabVIEW RIO architecture
Instrument Driver *FPGA Extensions*

- Embedded Controller (CPU)
- PCI Express
- Host FPGA
- Software-Designed Instrument (VST)

**Host Application**
- Instrument Driver API
- Vendor-Defined
- Application-Specific FPGA VI

**Application IP API**
- Application IP
- Data, Triggers, Device State

**Application IP API**
- Application IP API
Instrument Driver **FPGA Extensions**

**Host**

![Diagram of Instrument Driver and Application-Specific Host VIs]

- Instrument Driver
- Application-Specific Host VIs

**FPGA**

![Diagram of Instrument Driver FPGA VIs and Application-Specific FPGA VIs]

- Instrument Driver FPGA VIs
- Application-Specific FPGA VIs

FPGA ext.mask trigger
Software-Designed Instrument Architecture

User Application

Host Interface

Config. & Calibration
Waveform Acquisition
Waveform Generation
Sync.
Trigger

Instrument Design Libraries

Host Interface

Host
FPGA

ni.com
Instrument Design Libraries

- Color-coded and thicker VI border
- Bundled into Host and FPGA *.lvlib
- Located in [LabVIEW Dir]\instr.lib\n  - NI “owned,” but primarily open source
  - VIs are locked to avoid accidental editing
- Host and FPGA Palettes

Typical subVI

Instrument Design Library VI

NI PXIe-5644R

RF Input Con...
RF Output Con...
Basecard Con...
NI 5644R Con...
Multirecord...
Waveform S...
DSP
Register Bus
Embedded C...
Trigger Sync...
Basic Elements
FIFO
Memory

NI PXIe-5644R

RF Input Con...
RF Output Con...
Basecard Con...
Multirecord...
Waveform S...
Register Bus
Embedded C...
NI VST Calibr...
LabVIEW Sample Projects for Software-Designed Instruments

Completely flexible, built on instrument design libraries

**Instrumentation**
Implements triggering and multirecord acquisition and generation.
Provides a familiar look and feel to traditional instrument drivers on the host.

**Streaming**
Implements basic real-time streams to and from the host
Serves as a starting point for implementing real-time DSP and rerouting data streams between loops, FPGAs, and host processing.
Streaming Sample Project
VST Example

User Application

VST Streaming Sample Project

Host FPGA

RF Hardware

Instrument Design Libraries

ni.com
Record-Based Sample Project

VST Example

User Application

Simple VSA / VSG
Sample Project

Host
FPGA

RF Hardware

Instrument Design Libraries

ni.com
IP and Examples are Available

ni.com Community for IP and Examples

ni.com/vstgettingstarted » Download examples and application IP for the VST
Thank You!
Stay Connected During and After NI Technical Symposium

facebook.com/southernafica.ni

twitter.com/niglobal

youtube.com/niglobal

ni.com/niglobal